REMARKS

The specification has been revised to clarify/correct the grammar and to correct various self-evident errors in punctuation, figure identification, and reference symbol usage including the addition of several missing reference symbols. In several instances, references to figures have been moved to more appropriate places in the specification. Certain of the reference symbols have similarly been moved to more appropriate places in the specification. Minor non-substantive modifications to the specification have been made in some of the instances where reference symbols and references to figure numbers have been shifted to more appropriate locations in order to accommodate the shifts.

Some of the paragraphs in the fabrication description presented in paragraphs 95 - 112 of the specification have been divided into multiple paragraphs in order to make the fabrication description easier to read. As a result, the amended specification has more paragraphs than the originally filed specification. However, the paragraphs in the specification have not yet been renumbered. After the requested revisions to the specification have been approved by the Examiner and entered, Applicants' Attorney expects to submit a substitute specification that incorporates all the approved changes. Applicants' Attorney also expects to appropriately renumber the paragraphs in the substitute specification.

In addition to the preceding changes to the specification, the Background material of paragraph 4 has been clarified. The number of the second U.S. patent cited in the Related Art material of paragraph 9 has been corrected from "5,471,314" to "5,471,341".

Paragraph 25 of the specification provides that "Starting with all the transistors in their non-conductive conditions, selected ones of the transistors are sequentially bombarded with electrons according to an image pattern at a dosage and average energy that cause each selected transistor to enter its conductive condition" and then that "During the sequential electron bombardment of the selected transistors, all of the transistors are disabled". Since the selected transistors constitute part of the transistors, the selected transistors are disabled and cannot conduct current during the sequential electron bombardment of the selected transistors even though they are in their conductive conditions. To make this point clear, a sentence has been added to paragraph 25 after the sequential-electron-bombardment

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statement to provide that "Accordingly, the selected transistors do not yet conduct current even though they are in their conductive conditions".

The subject matter of paragraph 54 of the specification has been revised to explicitly describe the subpixel arrangement shown in Fig. 2, namely that each pixel consists of a two-dimensional array of rows and columns of subpixels. A sentence has been added at the end of paragraph 55 to explain the Gaussian-type curve shown in the right-hand side of Fig. 2.

The second sentence of paragraph 56 of the specification recites that "Twice the subpixel width is defined as the lateral dimension between centers of the two transistor gate elements (pitch) plus the lateral width dimension of the transistor gate element in the same lateral dimension" where the phrase "the same lateral dimension" has been corrected to "the same lateral direction". Because the material preceding the corrected phrase "the same lateral direction" does not explicitly recite a lateral direction which constitutes "the same lateral direction", an appropriate earlier-recited "lateral direction" has been introduced into the second sentence of paragraph 56 by further amending that sentence to recite that "Twice the subpixel width is defined as the lateral dimension between the centers of the two transistor gate elements (pitch) in a lateral direction plus the lateral width dimension of the transistor gate element in the same lateral direction".

A paragraph has been inserted between paragraphs 56 and 57 of the specification to explicitly describe the anti-aliasing benefits of the light modulator of the present invention. More particularly, "aliasing" refers to distortion of a continuous line due to the nature of a screen display as is well known in the display art. As is likewise well known in the display art, "anti-aliasing" refers to smoothening rough, jagged edges of curved and diagonal lines of a screen display. With the definition of "anti-aliasing" in mind, the use of subpixels in the light modulator of Fig. 1 combined with scanning the subpixels in the manner described in the specification material preceding the newly inserted paragraph provides anti-aliasing. The new paragraph briefly describes the meanings of "aliasing" and "anti-aliasing" and then explains how the use of subpixels combined with scanning them in the recited manner achieves anti-aliasing.

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The phrase "storage capacitor dielectric layer 41" in paragraph 78 of the specification has been changed to "a storage capacitor dielectric layer 41 of insulating polymer" in conformity with the recitation of "lower layer 41 of insulating polymer" in paragraph 81.

The descriptions of layers 41 and 45 in paragraph 81 have similarly been modified in conformity with the descriptions of layers 41 and 45 elsewhere in the specification.

In paragraph 85 of the specification, the sentence reciting that "Delta coating 59 of each selected TFT 204 charges (+) toward adjacently located collector potential V_{coll}" has been deleted because that sentence might imply that delta coating 59 of each selected TFT reaches collector potential V_{coll} at the indicated point whereas the voltage on delta coating 59 of each selected TFT 204 can actually reach a maximum value less than collector potential v_{coll}. This correction has been made explicit in paragraph 85 by amending the first sentence of that paragraph to recite that "Each delta coating 59 remains charged to the writing potential, i.e., less than or equal to collector voltage V_{coll}, until the deposited charge is erased by aerial electrons since there is no conducting discharge path". For the reasons given above for amending paragraph 25 to specify that "Accordingly, the selected transistors do not yet conduct current even though they are in their conductive conditions", the next-to-last sentence in paragraph 85 has been amended to recite that "Although there is a charge-induced electric field on the TFT channel regions causing TFTs 204 to be in their conductive conditions, there is no source current to charge liquid-crystal cell capacitors C_{LC} and storage capacitors C_S".

In the fabrication description given in paragraphs 95 - 112 of the specification, item 100 represents the photoresist created in each of seven processes for creating a patterned layer of photoresist. That is, item 100 represents an implementation of each of seven different photoresist layers having respective patterns 103 - 109. Inasmuch as the specification did not originally identify the points at which the seven implementations of photoresist layer 100 are removed, seven brief sentences have been inserted in the fabrication description to identify where photoresist layers 100 having patterns 103 - 109 are respectively removed in conformity with Figs. 6a - 6e, 7a - 7j, and 8a - 8k.

Substrate 10 constitutes the starting point for the fabrication process and, as disclosed in paragraph 95 of the specification, preferably consists of glass The recitation in paragraph 95 that the thickness of substrate 10 is 0.7 - 1.1 "μm" has been corrected to recite that the thickness of substrate 10 is 0.7 - 1.1 "mm" since, as would be clear to a person skilled in the display art, it would be unfeasible to start such a fabrication process with a substrate having a thickness in the vicinity of 0.7 - 1.1 μm.

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The recitations of reference symbols "71" and "701" in paragraphs 107, 108, and 112 of the specification have been deleted since no reference symbol "71" or "701" appears in the drawings. The wording of paragraphs 107, 108, and 112 has been appropriately modified to account for the deletion of reference symbols "71" and "701".

Turning to the drawings, the specification provides in paragraph 42 on page 15 that "FIGs. 8a - 8m are cross-sectional side views representing further steps, starting from the stage of FIG. 7j, in the process for manufacturing the light modulator of FIG. 1a according to the invention". The Notice, mailed 9 June 2004, to File Missing Parts of Nonprovisional Application, specifies that Figs. 8l and 8m "appear to have been omitted from the application". In the Response submitted 8 August 2004 in response to the Notice to File Missing Parts, Applicants' Attorney notified the PTO that Applicants' Attorney elected not to take action pursuant to options (I) and (II) presented in the "Notice to File Missing Parts of Non-Provisional Application - Filing Date Granted".

Accompanying this amendment is a Preliminary Amendment to the Drawings by which missing Figs. 8l and 8m are inserted into the application. For the following reasons, the material illustrated in Figs. 8l and 8m is supported in the application as filed. Consequently, the insertion of Figs. 8l and 8m into the application does not introduce new matter into the application.

Figs. 8l and 8m illustrate how the display fabrication process of Figs. 6a - 6e, 7a - 7k, 8a - 8m, 9a - 9d, and 10 - 13 transitions from the stage of Fig. 8 k to the stage of Fig. 9a. As originally filed, paragraph 105 of the specification recited that:

> As shown in FIG. 8k, delta layer 59 is coated with a liquid polymer material, such as PI2610 supplied by HD Microsystems, and cured at 350°C to a preferred film thickness of 1 - 1.5 μm to form an electrically insulating layer 60. A blanket layer 61 of chromium is sputter deposited over delta layer 59 to a preferred thickness of 300 nm.

Paragraph 105 then originally recited[1] that:

> As shown in FIG. 8l, chromium layer 61 is coated with a positive tone photoresist 100 and exposed to actinic light through a photomask, with alignment and optical registration to superimpose pattern 109 over previously defined gate dielectric layer 58, and subsequently developed by conventional

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[1] This sentence in paragraph 105 is being split into two sentences in order to make the specification easier to read. For the same reason, paragraph 105 is being divided into three paragraphs. One of the divisions in paragraph 105 occurs at this point.

means to define pattern 109 in resist 100 whereby portions of chromium layer 61 are uncovered.

Newly added Fig. 8l referred to in the foregoing part of paragraph 105 of the specification repeats Fig. 8k except that (a) Fig. 8l illustrates photoresist 100 having pattern 109 situated on top of chromium layer 61, (b) reference symbol "58" for the gate dielectric layers appears in Fig. 8l but not in Fig. 8k, and (c) reference symbol "60" for the insulating layer situated on delta coatings 59 formed on gate dielectric layers 58 appears in Fig. 8k but not in Fig. 8l. Since the formation of photoresist 100 with pattern 109 is described in paragraph 105, the material depicted in Fig. 8l is fully supported in the application as filed.

After describing the formation of photoresist 100 with pattern 109, paragraph 105 of the specification continues by reciting that[2]:

> The uncovered chromium is chemically etched in a commercially available etchant provided by Transene Chemicals or other vendor to remove chromium metal in the regions defined by pattern 109 to define collector grid 62, and to expose portions of insulating layer 60 in regions overlying gate dielectric 58. The exposed regions of layer 60 are etched by RIE, using oxygen plus fluoride ion gas chemistry, to remove the portions of polymeric insulating layer 60 in the regions not protected by collector electrode 62 to form collector insulator 63 as shown in FIG. 8m.

Newly added Fig. 8m referred to in the preceding part of paragraph 105 of the specification repeats Fig. 8l except that (a) the portions of chromium layer 61 and insulating layer 60 situated below the openings in photoresist 100 having pattern 109 as shown in Fig. 8l are absent in Fig. 8m, (b) the remainder of chromium layer 61 is labeled "62" in Fig. 8m to define the collector grid, (c) the remainder of insulating layer 60 is labeled "63" in Fig. 8m to define the collector insulator, (d) photoresist 100 having pattern 109 is absent in Fig. 8m, (e) reference symbol "59" for the delta coatings appears in Fig. 8m but not in Fig. 8l, and (f) reference symbol "58" for the gate dielectric layers appears in Fig. 8l but not in Fig. 8m.

The fabrication process continues with the release of display electrodes 31 and spacing elements 43 from mandrel substrate 20 as described in the material beginning with Fig. 9a and paragraph 106 of the specification. Fig. 9a repeats Fig. 8m except that (a) dry film photoresist 101 is situated on collector grid 62 to form sub-assembly 110 with grid 62 and the underlying structure, (b) reference symbol "63" for the collector insulator appears in

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[2] The second division of paragraph 105 occurs after the first sentence of this material.

Fig. 8m but not in Fig. 9a, (c) reference symbol "59" for the delta coatings appears in Fig. 8m but not in Fig. 9a, (d) reference symbol "20" for the mandrel substrate appears in Fig. 9a but not in Fig. 8m, and (e) a reference symbol "700" appears in Fig. 9a but not in Fig. 8m[3].

Photoresist 100 having pattern 109 does not appear in Fig. 9a. This shows that photoresist 100 having pattern 109 is, as indicated by the absence of this photoresist in Fig. 8m, removed between the stage of Fig. 8l and the stage of Fig. 9a[4]. Since the removal of the portions of chromium layer 61 and insulating layer 60 below the openings in photoresist 100 having pattern 109 is described in paragraph 105, the material depicted in Fig. 8m is fully supported in the application as filed.

Insertion of Figs. 8l and 8m into the application helps make the fabrication process easier to understand. Inasmuch as the material illustrated in both of Figs. 8l and 8m is fully supported in the application as filed, it is appropriate to add Figs. 8l and 8m to the application in order to make the application easier to read.

Turning to the claims, two of the original claims were numbered "55". The second-numbered Claim "55" has been changed to Claim "56" to eliminate the duplicate-numbering error in the claims. Claims 1, 12, 15, 17, 23, 27, 28, 41, 44, 46, 51, 53, 55, and 56 have been amended to clarify the claimed subject matter and correct various self-evident errors. No claims have been added or canceled. Accordingly, Claims 1 - 58 are now pending.

Claims 1 - 30 are structure claims while Claims 31 - 58 are method claims. Applicants' Attorney notes that, in response to the Restriction Requirement mailed 13 September 2005, structure Claims 1 - 30 are provisionally elected for prosecution in this application via the accompanying Response to Restriction Requirement. Applicants' Attorney therefore expects that the Examiner will withdraw method Claims 31 - 58 from examination in this application. The application is in suitable condition for examination of structure Claims 1 - 30.

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[3] Reference symbol "700" does not appear in the specification. Accordingly, reference symbol "700" is being removed from Fig. 9a via the accompanying Preliminary Amendment to Drawings.

[4] Paragraph 105 is being amended to explicitly recite that photoresist 100 having pattern 109 is removed after the patterning of chromium layer 61 and insulating layer 60 to respectively form collector grid 62 and collector insulator 63.

Please telephone Attorney for Applicant(s) at 650-964-9767 if there are any questions.

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